LINEAR TECHNOLOGY

DESIGN NOTES

Addressable I²C Bus Buffer Provides Capacitance Buffering, Live Insertion and Nested Addressing in 2-Wire Bus Systems

Design Note 329

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Introduction

In an effort to improve the reliability of large data processing, data storage and communications systems, their subsystems include a growing number of active circuits to monitor parameters such as temperature, fan speed and system voltages. Individual subsystem monitors often communicate with the host system through 2-wire serial busses, such as SMBus or I²C™, to a dedicated microcontroller.

As monitoring functions increase in complexity and number, several practical problems arise. First, data bus rise time specifications become difficult to meet. Second, many uninterruptible systems cannot tolerate cycling power whenever a new I/O card is installed. Finally, a device's address is often dictated by the function that it performs. If an existing system already contains a temperature sensor, for example, then inserting a new I/O card with a temperature sensor risks having two devices with the same address. The new LTC®4302-1/LTC4302-2, addressable 2-wire bus buffers provide solutions to all of these problems.

Live Insertion and Removal and Capacitance Buffering Application

The LTC4302 solves bus connect/disconnect problems by creating an active bridge between two physically separate 2-wire busses. The LTC4302's two "input" pins, SDAIN and SCLIN, connect to one 2-wire bus, i.e., a backplane; and its two "output" pins, SDAOUT and SCLOUT, connect to a second 2-wire bus, i.e., an I/O card.

The application shown in Figure 1 highlights the live insertion and removal and the capacitance buffering features of the LTC4302 -1. Because the LTC4302's SDA and SCL pins default to a high impedance and low capacitance (<10pF) state even when no V_{CC} voltage is applied, an LTC4302 can be inserted onto a live 2-wire bus without corrupting it.

If a staggered connector is available, make CONN the shortest pin and connect a large value resistor from CONN to ground on the I/O card to force the CONN voltage low before it connects to the backplane. This ensures that the LTC4302 remains in a high impedance state while SDAIN and SCLIN are making connection during live insertion.

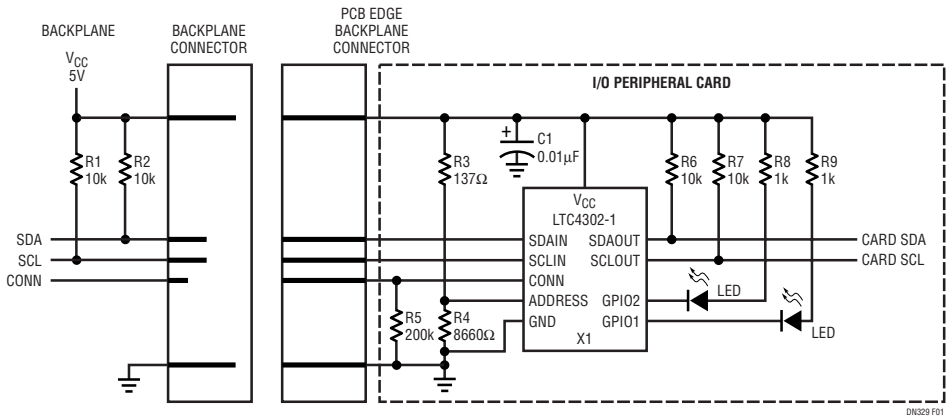

Figure 1. LTC4302-1 in a Live Insertion and Capacitance Buffering Application

With the I/O card firmly connected, drive CONN high to allow masters to communicate with the LTC4302. During live removal, having CONN disconnect first ensures that the LTC4302 enters a high impedance state in a controlled manner before SDAIN and SCLIN disconnect.

Inserting an LTC4302 on the edge of the card isolates the card capacitance from the backplane. As more I/O cards are added to the system, placing an LTC4302 on the edge of each card breaks what would be one large, unmanageable bus into several manageable segments. Moreover, the LTC4302 can be programmed to provide rise time accelerator pull-up currents on all four SDA and SCL pins during rising edges, to further aid in meeting the rise time specification. Figure 2 shows the rise time improvement achieved for V_{CC} = 3.3V and bus equivalent capacitances of 50pF and 150pF.

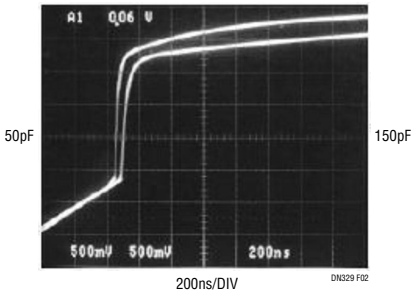

Figure 2. Rise Time Accelerators Reduce Rise Time for C_{BUS} = 50pF, C_{BUS} = 150pF

Nested Addressing and 5V to 3.3V Level Translator Application

Figure 3 illustrates how the LTC4302 can be used to expand the number of devices in a system by using nested addressing. In this example, each I/O card contains a sensor device having address 1111 111. The LTC4302 isolates the devices on its card from the rest of the system until it is commanded to connect by a master. If masters use the LTC4302s to connect only one I/O card at a time, then each I/O card can have a device with address 1111 111 without any conflicts.

Figure 3 also shows the LTC4302-2 providing voltage level translation from the 5V backplane SDA and SCL lines to the 3.3V I/O card lines. The LTC4302-2 functions for voltages ranging from 2.7V to 5.5V on both V_{CC} and V_{CC2}. If either V_{CC} or V_{CC2} supply voltage falls below its UVLO threshold, the LTC4302-2 disconnects the backplane from the card so that the side that is still powered can continue to function.

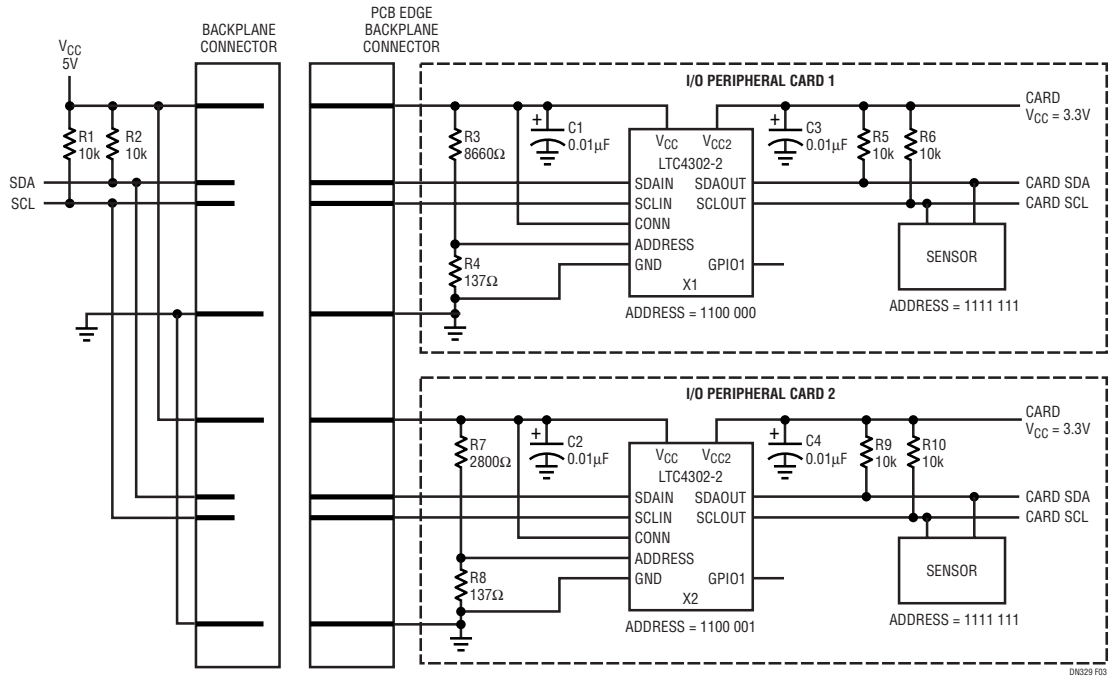

Figure 3. LTC4302-2 in a Nested Addressing and 5V to 3.3V Level Translator Application

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